A New Semiconductor-Wafer Market Based on the Deepening of Natural Surface Undulations to Form Strongly Textured Atomic Ridges (STAR) With Pitches from 0.6 to 5.4 nm: Model Demonstrations in the Physical and Life Sciences

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ABSTRACT

A broad patent position has been established for semiconductor wafers with physically-deepened grooves, ridges and dots on particular crystal planes with perfect pitches of 0.9 to 5.4 nm. Optical lithography is used in a standard production facility on top of deepened natural underlying nanotexture to produce quite useful new devices and ICs. See www.starmega.com. The very high value-added com-ponent of these wafers is the business opportunity. One method for producing nanoridges on any crystal surface (including III-Vs) will be discussed. Several applications will be demonstrated with mock-ups: ballistic transport; ultra-low-power MOSFETs; low-cost simultaneous sensing of hundreds of different molecules based on arrays containing nanotubes, DNA, and/or other molecules; high temperature BCS superconductors (not "HTS") with Buckyballs between flexible walls; mega-tip nanoprobes; particle filters with openings down to 0.3 nm for nano-shadow masks and for oxygen enrichment of air.

Keywords: silicon and III-Vs, ballistic transport, nano-mosfets, security sensors, superconducting interconnects

1 PERSPECTIVE

The ability to produce nanometer width grooves and ridges in a single crystal surface opens up a multitude of structural permutations and applications. This is demonstrated in Figure 1, which shows a pair of atomic ridges surrounding an interposed nanometer-width groove. This particular structure is relatively simple to produce over large areas and allows a sort of ballistic transport of electrons in the ridges while a normal inversion layer of electrons exists just below the ridges. The mobility of the highly scattered electrons in such an inversion layer of a MOSFET is typically about 500 cm^2/Vs, which leads to an average drift velocity of about $5X10^5$ cm/s in a large transistor of 10 μm length between the source and drain (S-D). By contrast, we estimate that the velocity of the electrons in the narrow ridges can reach a velocity of about $5X10^7$ cm/s since they suffer essentially no lateral scattering in the ridges [1].

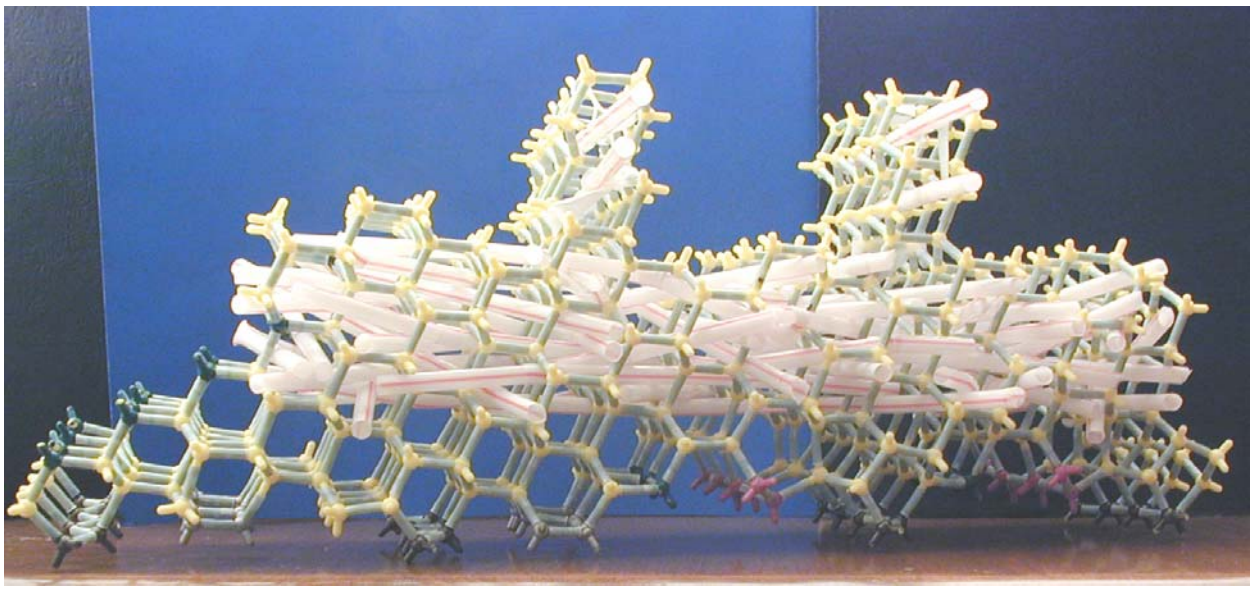

Figure 1: Electron waveguides in parallel with a normal nMOSFET on a ridged (3 3 7) wafer with a 1.57 nm pitch. Source-to-drain current flows into the plane of the figure. The gate conductor and dielectric are omitted for clarity. The (5 5 12) surface with 5.4 nm unit cell is on the bottom of the model. A segment of a {001} surface is shown at the left edge facing up.

We have chosen a large nMOSFET in the example above and a small S-D voltage of only 1V between the source and drain to emphasize one of the strong advantages of such structures for electronic devices, namely the potentially very large increase in the velocity of the electrons in the atomic ridges. The electrons in the inversion layer will have a wide distribution of velocities due to scattering of several types. The plastic straws in the atomic model illustrate the chaotic trajectories of the electrons in the normal inversion layer and the almost un-scattered trajectories in the narrow ridges.

In addition, the "Smallest Meaningful Dimension" (SMD) of only 0.31 nm in the above example allows fabrication of devices and circuits exhibiting reliable and useful quantum effects at room temperature and even far above. Furthermore, it does this using today's optical technology to make otherwise standard-looking MOSFETs piggybacked on STAR wafers. This is in sharp contrast to most of the research devices presently being fabricated using the best modern lithographic methods (e-beam, x-rays, EUV). The latter are generally limited in their SMD to 20 to 50 nm and their research devices must often be operated at very low temperatures of less than 4K. This follows from the fact that the first excited level $\_E_1$ of a deep potential well depends inversely on the square of the width, **w**, of the well [2], namely:

$$\_E_n = n^2 K / (w^2 m_r^*) \ , \qquad (1)$$

where $n = 1, 2, 3$…, **w** is the width of the well, m_r^* is the conductivity effective mass of the electron relative to the rest mass of the electron (which is about 0.26 for an electron in Si), and **K** includes well known constants and is 0.38 eV nm^2 when **w** is in nm. Since the STAR patents [3-6] cover groove and ridge widths for Si from 0.6 to 5.1 nm (and pitches from 0.94 to 5.35 nm), it is easy to show that the first energy level of 0.056 eV at room temperature of 300K (27°C) is active even in the ***largest*** ridge of 5.1 nm. Since the thermal energy, kT, at 300K is only 0.026 eV, this is not enough to smear out the quantum effects of even this largest nano-ridge. At the smallest attainable stable ridge width of 0.31 nm shown in Figure 1, the first level is at about 15 eV so the devices should operate at ***much*** higher temperatures reaching in principle above the melting point of Si. The III-V compounds often have smaller effective masses than Si, so ridges and grooves in these materials may operate at even higher temperatures.

We should also point out here that even a very shallow potential well of a depth of just one atom still has bound excited states. The energy levels can be shown to be smaller than the values given for the deep well above by a factor of π^2 (about one magnitude). Thus, our narrowest ridges and grooves of 0.3 to 0.6 nm can still give robust quantum effects at room temperature at depths as small as one or two atoms.

2 ONE GENERIC TECHNOLOGY

Before discussing several of the many other diverse applications for the STAR structures, we will review one generic technology for obtaining nm-width grooves on Si wafers (which will also be applicable to many other crystalline materials). We start with a wafer of any diameter that has been X-ray aligned in the desired direction, sawed, and chem-mechanically polished (CMP) in a standard Si wafer facility [7]. The wafer is then heated in a UHV system to about 1150°C for a minute at a pressure less than 10^{-10} torr to remove the native oxide and impurities and to allow the surface to restructure. It is then slowly cooled to room temperature, where it can have "pre-assembled" precise values of pitch ranging from 0.94 to 5.35 nm. The ***clean*** surfaces are the (1 1 4) and the (5 5 12), which produce large regions of perfectly straight atomic ridges with pitches of 1.63 and 5.35 nm, respectively [8]. After reaching room temperature or some other suitable substrate temperature where the arriving atoms will have a sufficiently low surface diffusion coefficient, an etch resistant material is evaporated onto the surface at near grazing incidence so that only the surface atoms that are slightly elevated above the neighboring atomic undulations are coated. The sample is generally rotated during this procedure to avoid the formation of needles pointing to the evaporation source and to form relatively tall vertical etch masks of say 5 to 20 atoms height to serve as a mask against a subsequent chemical or an ion beam etching process [3,4]. The latter etching process is continued until the desired groove depth is obtained, which may only require the removal of a single atom or may proceed for thousands of atoms with highly anisotropic etching processes. An example of the natural undulating surface ***before*** both the evaporation and the etching processes is apparent from the bottom of Fig. 1 for the (5 5 12) surface which has repeating elevated ridges about 0.3 nm higher than the undulations between the ridges. A directed evaporation at about 1 to 5 degrees from grazing is adequate to insure that very little material is evaporated in the regions between the ridges, and the rotation of the wafer doesn't change the situation to any significant degree [10]. In many cases, this wafer can be submitted to a standard foundry where it is handled exactly like a standard Si wafer to produce decidedly non-standard devices and ICs.

Alternatively, in order to obtain other precise pitches, the high index Si surfaces may have an added evaporation of a very thin layer of a metal such as Au, Ga, or Ag followed by a UHV heat treatment to cause the surface to facet and

restructure to particular favored crystal surfaces. ***(A "high index surface" is defined as one having at least one of its Miller indices greater than 1. The (1 1 2) qualifies, as does the (5 5 12). The latter is often informally called the "(1 1 2.4)" to make it clear that it is about halfway between the (1 1 2) and the (1 1 3) planes.)*** This allows a wide selection of precise pitches at particular values of 0.94, 1.57, 1.63*, 1.91, 2.21, 2.51, 3.14, 3.45, 3.78, and 5.35* nm, where the asterisks denote the clean surfaces mentioned earlier. All of the above high index surfaces are attainable and they can be all be considered as (1 1 X) planes if X is allowed to have non-integer values. For example, the 1.91 nm pitch is the surface unit cell of the (5 5 7) plane, or informally the "(1 1 1.4)" surface.) The ones without asterisks usually require the deposition of a sub-monolayer or monolayer ML thickness of some metal and a UHV heat treatment [4,9].

A good example of the above process involves the smallest attainable pitch with stable groove walls, which is generally the (1 1 2) surface with a ***sub-nanometer*** surface unit cell of 0.94 nm which is produced using a single ML of Ga and a heat treatment at about 450 C. If the Ga layer is not present, the clean (1 1 2) surface after a UHV heat treatment consists of many (111) and (113) facets, and the Ga layer causes it to "unfacet" to form an atomically flat (1 1 2) surface [11]. By contrast, ***an exactly opposite result*** can be obtained by coating an atomically flat clean (5 5 12) wafer (as shown in Fig. 2) with as little as 0.05 ML of Au and heating it to 900C. This sub-ML film of Au causes it to form relatively large facets of the (7 7 15) surface with interspersed (1 1 3) facets (as shown in Fig. 3) [4,9]. Of course, if one ***starts*** with a wafer precisely aligned on the (7 7 15) surface, its initial condition is a faceted surface after a UHV heat treatment until the small amount of Au is added and heated to 800C. After this Au process, it becomes a large atomically flat (7 7 15) surface with ridges with precise and perfectly regular pitch (as in the large facets of Fig. 3).

The ability to attain in a controlled manner such a large number of specific values for the precise pitch in the (partial) list above is a very important aspect of the STAR wafer technology. For example, it allows the fabrication of whole wafers with nanowidth grooves designed to encase a particular diameter of DNA, Buckyball, or nanotube, or a particular spacing between electrons and holes in a new type of surface emitting laser, etc.[3]. Actually, the groove widths have much more variability of choice than do the pitch values. This is because the wall thicknesses can be chosen to be essentially any integer value of the "***Single Channel Wall Thickness"*** (SCWT) shown in Fig. 1. An example of this is shown in Fig. 4 below where Buckyballs are inserted between two double-SCWTs. They can also be inserted between single SCWTs for greater flexibility [3]. We believe this will be an important factor in the attainment of a good high temperature superconductor with Bardeen-Cooper-Schreiffer (BCS) character as opposed to the typical HTS type superconductors. The possibility exists that zero-loss interconnects for ICs may be developed that operate above liquid nitrogen temperature. Please note that the Buckballs stack in the flexible walls as if the walls were not present, something like ordered marble layers with thin plastic food wrap interlayers.

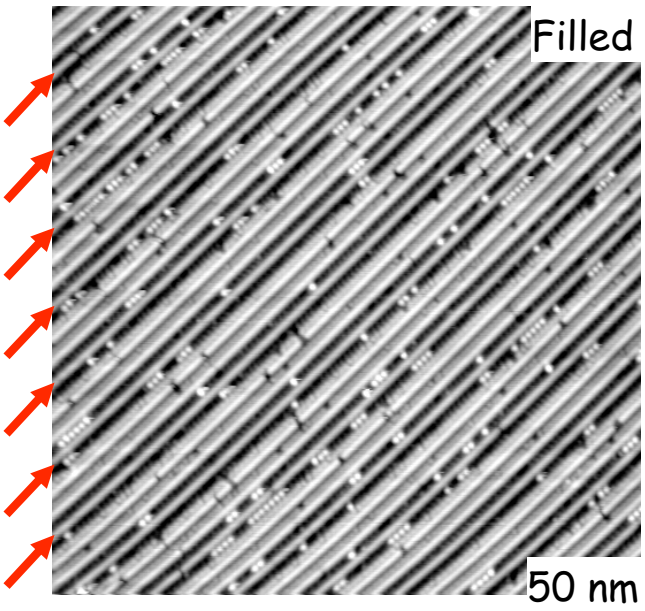

Figure 2: A clean (5 5 12) surface with the arrows showing the regular 5.35 nm spacing [4].

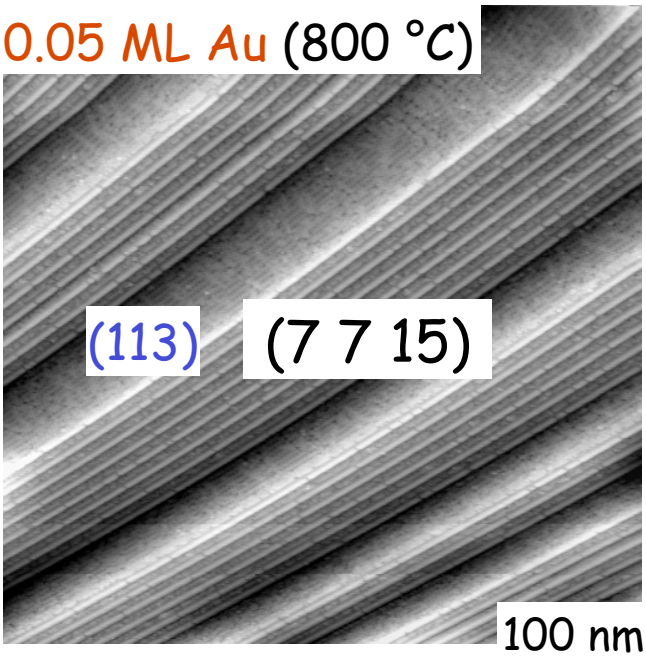

Figure 3: The restructured (5 5 12) surface showing the alternating (7 7 15) and (1 1 3) facets after adding 0.05 ML of Au and UHV heating at 800C. The atomic ridges on the (7 7 15) have a perfect pitch of 3.45 nm [4].

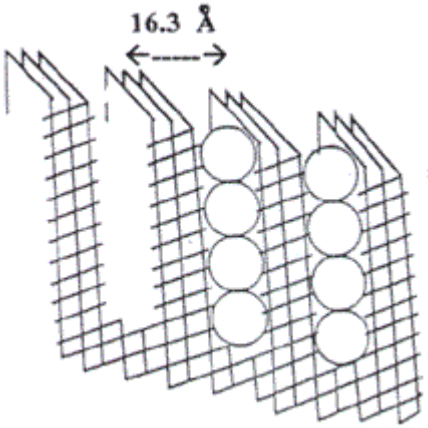

Figure 4: Buckyballs in a (1 1 4) nano-grooved surface [3].

We invite the interested reader to visit our website at www.starmega.com. where we discuss and have LINKS to all four of the STAR patents. In particular, we discuss the very low power MOSFET operating at an S-D voltage of about 0.5 V that will have a very high electron velocity [1,3]. We also discuss a cantilever mega-tip array on nm-width pitch for SCULPTING true arbitrary nm geometry circuits and other applications [5].

We also propose a radical type of ultra-thin filter based on STAR technology merged with a SIMOX-type process [6]. A detailed fabrication technology is presented which produces openings down to at least 0.3 nm in width on a regular nm-pitch array. These ultra small openings can be made to cover large Si wafers for use as shadow masks for either charged or uncharged particles for many tasks, including a nano-lithography scheme, and a means for passively separating oxygen from normal air. The latter could provide an oxygen deficient patient with a means to produce oxygen enriched air without carrying a heavy oxygen tank.

Finally, we invite the attendees at the Nanotech 2004 in Boston conference to visit our Exhibitors Booth #102 in the Grand Ball Room at the Sheraton Boston on Tuesday and Wednesday, March 8 and 9 to ask questions about the technical and investment possibilities.

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